100 nm Gate Length High Performance / Low Power CMOS Transistor Structure

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Abstract

We report a very high performance 100nm gate length CMOS transistor structure operating at 1.2-1.5V. These transistors are incorporated in a 180nm logic technology generation. Various process enhancements are incorporated to significantly improve transistor current drive capability relative to the results published in [1]. Unique transistor features responsible for achieving high performance are described. NMOS and PMOS devices demonstrate drive current of 1.04 mA/µm and 0.46 mA/µm respectively at 1.5V and 3nA/µm I_{OFF}. These are the best drive currents reported to date at fixed I_{OFF}. They represents 10% drive current improvement for both NMOS and PMOS devices relative to the results published in Ref.[1] without any change in gate-oxide thickness. High performance is demonstrated down to 1.2V. Inverter delay of less than 10 psec is reported at 1.5V at very moderate I_{OFF} values.

Introduction

CMOS technology dimensions are being aggressively scaled to meet historic microprocessor performance improvement trends. In addition, there has been concurrent scaling of supply voltage with device dimensions to keep power manageable and meet reliability requirements. The transistor structure described in this paper supports poly gate length of 100nm and demonstrates very high drive current at reduced power supply (1.2-1.5V) and low I_{OFF} (3nA/um). Key features incorporated in the transistors which are responsible for demonstrating high performance include (a) insertion of a "Notched-Poly" process (b) implant and anneal optimization (c) 2nm physical gate oxide thickness [3nm electrical T_{ox}^{inv}] and (d) change from Titanium to Cobalt salicidation process. These features are discussed in detail in the following section.

Transistor Features

(a) Poly Profile Engineering: A unique transistor feature which intentionally creates a notch at the bottom of the poly gate was introduced as illustrated in Figure 1. This feature enables a reduction in the total gate capacitance by reducing the gate length dimension at the poly-Si/gate-oxide interface. The poly-Si dimension at poly-Si/gate-oxide interface is 100nm for the devices reported in this work. By offsetting the source-drain-extension (SDE) implant from interface, higher SDE implant dose is incorporated while independently minimizing C_{MILLER}. This is illustrated in Figure 2. This results in lower parasitic resistance and hence higher drive current at low C_{MILLER}. Figure 3 shows the normalized drive current dependence on C_{MILLER} for NMOS and PMOS devices. C_{MILLER} was varied by changing the poly notch dimension. These data demonstrate that high drive current can be maintained at low C_{MILLER} by employing the notched-poly process. The minimum SDE to gate overlap was selected based on providing sufficient process margin to the drive current degradation cliff [2]. The nominal C_{MILLER} target is 0.27 fF/µm for NMOS and 0.24 fF/µm for PMOS transistors reported in this work. A tight control of poly-notch dimension is necessary for incorporating this feature into logic products. Figure 4 demonstrates a constant NMOS C_{MILLER} vs. poly pitch behavior, which indicates uniform poly notch from isolated to nested poly lines.

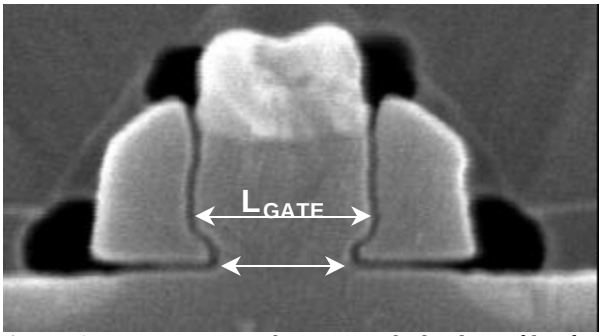

Fig. 1. SEM cross-section showing notched poly profile of a fully processed device. L_{GATE} is larger than the poly dimension at the poly-Si/gate-oxide interface.

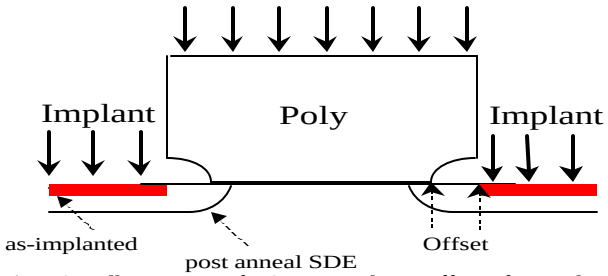

Fig. 2. Illustration of SDE implant offset from the poly-Si/gate-oxide interface due to presence of poly notch.

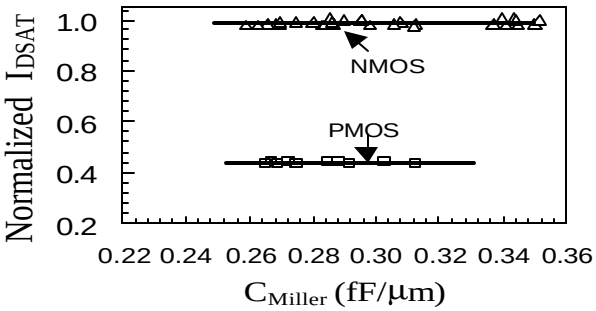

Fig. 3. Normalized drive current dependence on C_{MILLER} by modulating poly notch (all drive currents normalized with respect to NMOS drive current with largest C_{MILLER}).

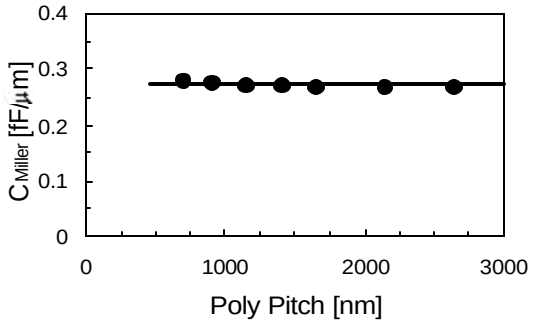

Fig. 4. NMOS C_{MILLER} vs. poly pitch for notched poly process.

b) Well-Halo and SD-Extension Engineering: In order to achieve high drive current, extremely aggressive well/halo engineering was employed. Low energy arsenic and boron implants were used to form shallow source-drain extensions. Retrograded Indium and Arsenic wells were used for NMOS and PMOS devices respectively. Angled halo implants, performed post gate formation, were employed to minimize the drive current degradation between the worst case and the nominal poly dimensions. A plot of NMOS short channel threshold voltage roll-off characteristics is shown in Figure 5. A hump in the characteristic is attributed to the well doping dependence on gate length for these halo devices. The worst case device was carefully targeted to be at the peak of the hump. As a consequence, the threshold voltage for the nominal device is lower than the worst-case device. This increases the gate drive (V_{CC}-V_T) for the nominal device, which results in higher linear and saturated drive current (I_{DSAT}) relative to both a non-halo and an un-optimized halo device. The gain in nominal I_{DSAT} is >10% relative to a non-halo device.

c) 2nm Physical Gate-Oxide: In order to achieve high drive current and minimize short channel effects a gate oxide process with 2 nm physical thickness (3 nm electrical T_{ox}^{inv}) was developed which meets performance, reliability and manufacturability criteria. High electron and hole mobilities are required to achieve high linear and saturated current drive. The measured mobility dependence on the effective field, shown in Figure 6, demonstrates that high electron and hole mobilities can be achieved for gate oxide

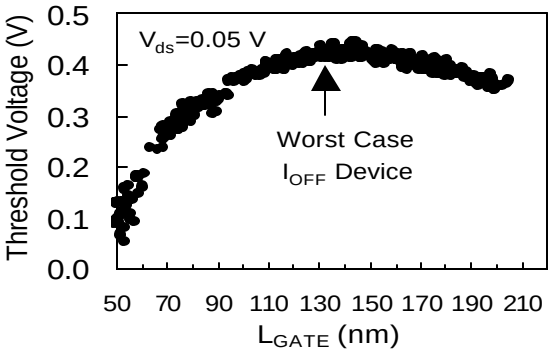

Fig. 5. NMOS threshold voltage vs. L_{GATE}.

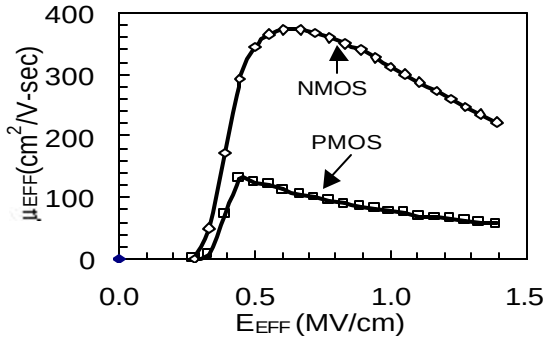

Fig. 6. Effective electric field dependence of electron (NMOS) and hole (PMOS) mobilities for 2nm physical gate oxide.

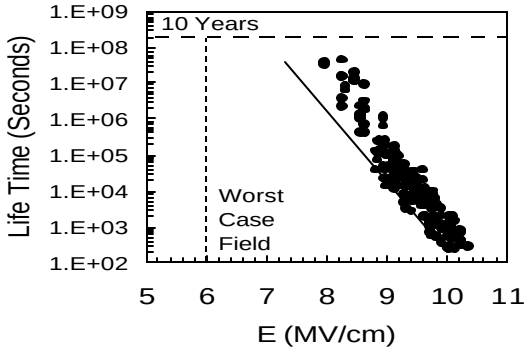

Fig. 7. 2nm gate oxide TDDB at 125C from capacitor data.

with 2 nm physical thickness. Reliability of ultra-thin gate oxide is a major concern. As shown in Figure 7, the dielectric time to fail for the 2nm physical gate oxide, fabricated in this work, exceeds the requirement for 1.5V operation with allowed tolerance.

d) Junction Capacitance Minimization: Special emphasis was placed on minimizing junction capacitance to improve performance and reduce active power. Low N+ and P+ area junction capacitance values of 0.6 and 0.8 fF/μm^2 at 0V bias are achieved without compromising isolation design rules.

e) Salicidation: $TiSi_2$ process [1] was replaced with $CoSi_2$ for the devices reported in this paper. As shown in Figure 8, the nominal sheet resistance is below 4 Ω/sq. while

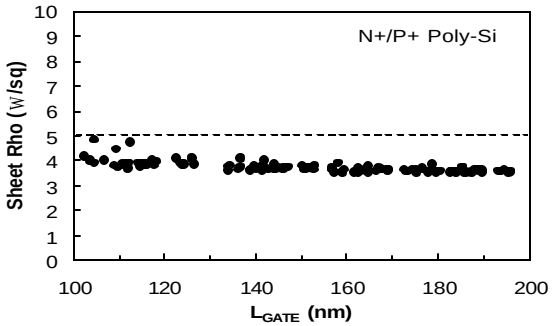

Fig. 8 $CoSi_2$ sheet resistance vs. poly-Si line width.

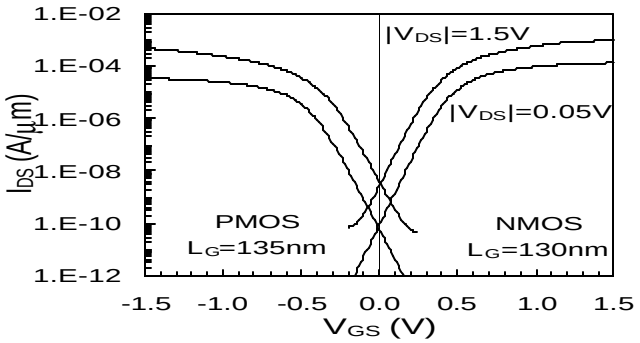

Fig. 9 MOSFET subthreshold curves.

TABLE1	Ref. [1]	This Work		
V_{DD} (V)	1.5	1.5	1.2	1.2
L_{GATE} (n) [nm]	130	130*	130*	130*
L_{GATE} (p) [nm]	150	135*	135*	135*
T_{ox}^{inv} (n) [nm]	3.0	3.0	3.0	3.0
T_{ox}^{inv} (p) [nm]	3.0	3.0	3.0	3.0
I_{DSAT} (n) [mA/μm]	0.94	**1.04**	**0.76**	**0.82**
I_{DSAT} (p) [mA/μm]	0.42	**0.46**	**0.31**	**0.34**
I_{OFF} [nA/μm]	3	**3**	**3**	**10**
C_{JA} (n) [fF/μm^2]	0.65	0.6	0.6	0.6
C_{JA} (p) [fF/μm^2]	0.8	0.8	0.8	0.8
C_{Miller} (n) [fF/μm]	0.27	0.27	0.27	0.27
C_{Miller} (p) [fF/μm]	0.24	0.24	0.24	0.24
CV/I (n) [psec]	1.8	1.65	1.81	1.68
CV/I (p) [psec]	4.2	3.78	4.5	4.10
Energy-Delay product (n) [10^{-27} J-sec]	1.61	1.45	1.01	0.94

Table1. Summary of transistor characteristics reported in this work.
* These L_{GATE} values correspond to 100nm for NMOS and 105nm for PMOS at poly-Si/gate-oxide interface.

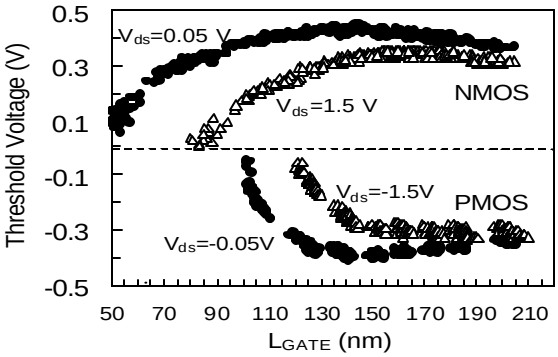

Fig. 10 NMOS and PMOS threshold voltage vs. gate length.

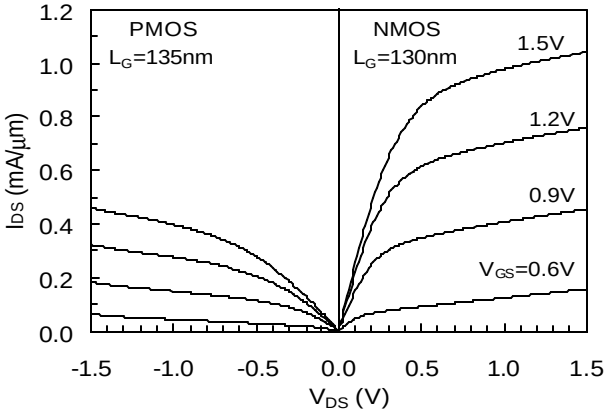

Fig. 11 MOSFET I-V curves.

worst case sheet resistance of 5 Ω/sq. is maintained for poly-Si line widths down to 100nm for poly-Si lines with alternating N+ and P+ doping.

Transistor Performance and Reliability

Transistor performance characteristics are summarized in Table 1. NMOS and PMOS short channel characteristics are well controlled as evident from less than 90mV/decade subthreshold slopes at L_{GATE} of 130nm and 135nm for NMOS and PMOS devices respectively (Figure 9). These corresponds to 100nm gate length for NMOS and 105nm for PMOS at poly-Si/gate-oxide interface. Short channel threshold voltage roll off characteristics are shown in Figure 10. Threshold voltage at 1.5V drain bias are 0.29V for NMOS at 130nm L_{GATE} and -0.23V for PMOS at 135nm L_{GATE}. Saturation drive currents at 1.5V are 1.04 mA/μm for NMOS and 0.46 mA/μm for PMOS (at 3nA/μm I_{OFF}) at these L_{GATE} targets (Figure 11). These results represent 10% drive current increase relative to the

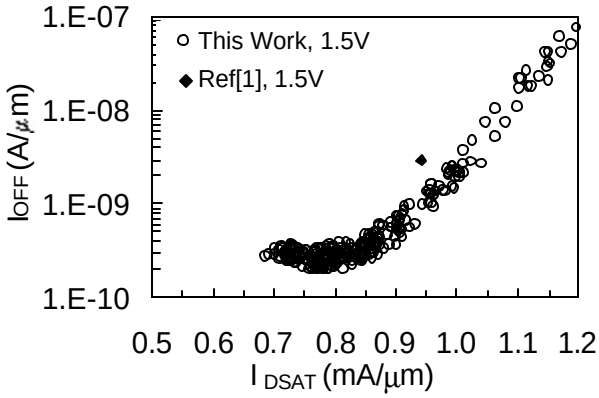

Fig. 12 NMOS drive current vs. off current.

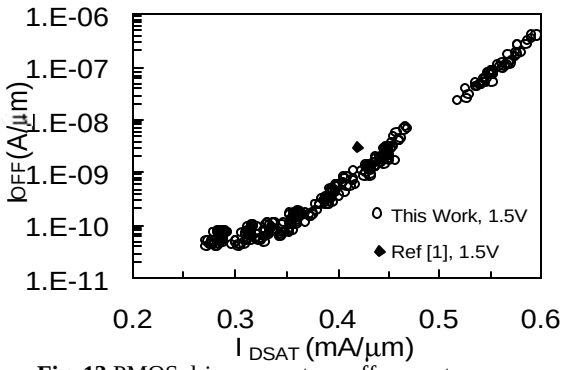

Fig. 13 PMOS drive current vs. off current.

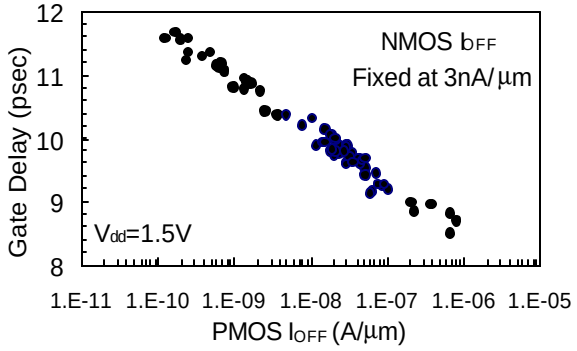

Fig. 14 Inverter gate delay per stage vs L_{GATE}, FO=1.

results published in Ref. [1] and have been achieved without any change in physical gate oxide thickness. NMOS and PMOS I_{DSAT} vs. I_{OFF} characteristics (Figures 12 and 13) show an improvement over our previous work [1] and are better than any other published bulk or SOI device. Table 1 also summarizes NMOS and PMOS performance at 1.2 V at 3nA/µm and 10nA/µm I_{OFF} criteria. High NMOS and PMOS drive current values of 0.76 mA/µm and 0.31 mA/µm respectively are obtained at 1.2V and 3nA/µm I_{OFF}.

Using 2.5% linear drive current degradation criteria for NMOS hot electron stress under worst case conditions and accounting for AC effects, the NMOS hot carrier lifetime exceeds 10 years for devices fabricated in this work.

Performance Metrics

Transistor gate delay, estimated using a CV/I metric, is 1.65 psec and 3.78 psec for NMOS and PMOS devices respectively at 1.5V. Figure 14 shows measured inverter gate delay vs. PMOS I_{OFF} for unloaded ring oscillator (fan out=1) operating at 1.5V at room temperature. NMOS I_{OFF} is fixed at 3nA/µm for these devices. The delay per stage at 1.5V falls below 10 psec when PMOS I_{OFF} is above 10nA/µm.

Power consumption is a growing concern for high performance microprocessors with increasing clock frequency and transistor count. A metric which comprehends both power and speed is the energy-delay product [3]. Figure 15 shows the estimated NMOS energy-

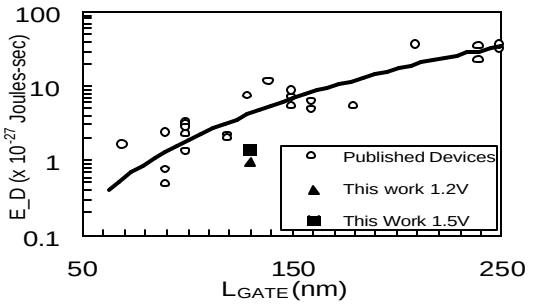

Fig. 15 NMOS Energy-Delay product.

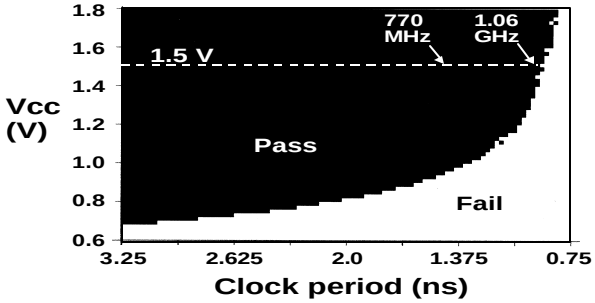

Fig. 16 F_{MAX} schmoo plot at room temperature for 16 Mbit SRAM.

delay product for a large number of published devices [3] and for the devices reported in this work. As evident from Figure 15, the NMOS energy-delay product metric is better than the published industry trend.

A 16Mbit CMOS SRAM has been designed and fabricated as a yield and reliability test vehicle for this technology [1]. Figure 16 demonstrates that the SRAM operates at 1.06 GHz at 1.5V [4].

Conclusion

In conclusion a high performance/low power 100nm gate length CMOS transistor is described with highest reported drive current to date at fixed I_{OFF}. Key technology features responsible for achieving the high performance at 1.2-1.5V supply are described. Inverter delay of less than 10 psec is reported at 1.5V at very moderate I_{OFF}. This transistor structure is incorporated in a 180nm logic technology generation.

Acknowledgement

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